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(43) Date of A Publication 30.08.2000

(21) Application No 9904007.3

(22) Date of Filing 22.02.1999

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(51) INT CL⁷
H04B 1/30 // H03L 7/00

(52) UK CL (Edition R)
H3A ALX AL2DX AL3X AXX
H4P PAO
U1S S2204 S2205 S2215

(56) Documents Cited
GB 2158330 A US 4944025 A

(58) Field of Search
UK CL (Edition Q) H3A AD AN AXB AXC AXD AXF
AXX
INT CL⁶ H03D , H03J , H04B
Online: WPI, JAPIO, EPODOC

(54) Abstract Title
Receivers

(57) In a receiver, AC coupling 12, 13 used to remove unwanted DC at the output of a mixer 4 introduces a notch into the centre of the IF pass-band and the carrier term is removed. This is overcome by comparing at 83 the DC component in the demodulator 6 output with a non-zero reference signal from 81 to apply an offset control signal to the mixer oscillator 5 so that the carrier term occurs at this offset frequency and not within the DC notch. The signal received by the demodulator 6 may be an FM signal or an IQ data signal. A phase lock loop 9 enabling initial tuning of the oscillator 5 is disabled when the demodulator 6 output equals the offset value. The oscillator is thereafter controlled by an AFC loop. In a further embodiment (fig.2 not shown), the baseband signal at mixer 4 output is upconverted before being demodulated. The receiver may form part of a transceiver.

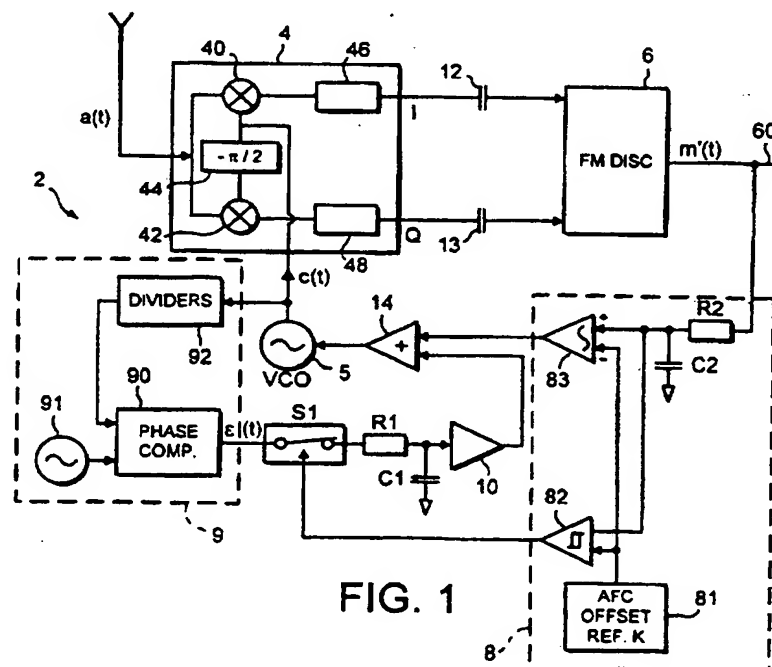
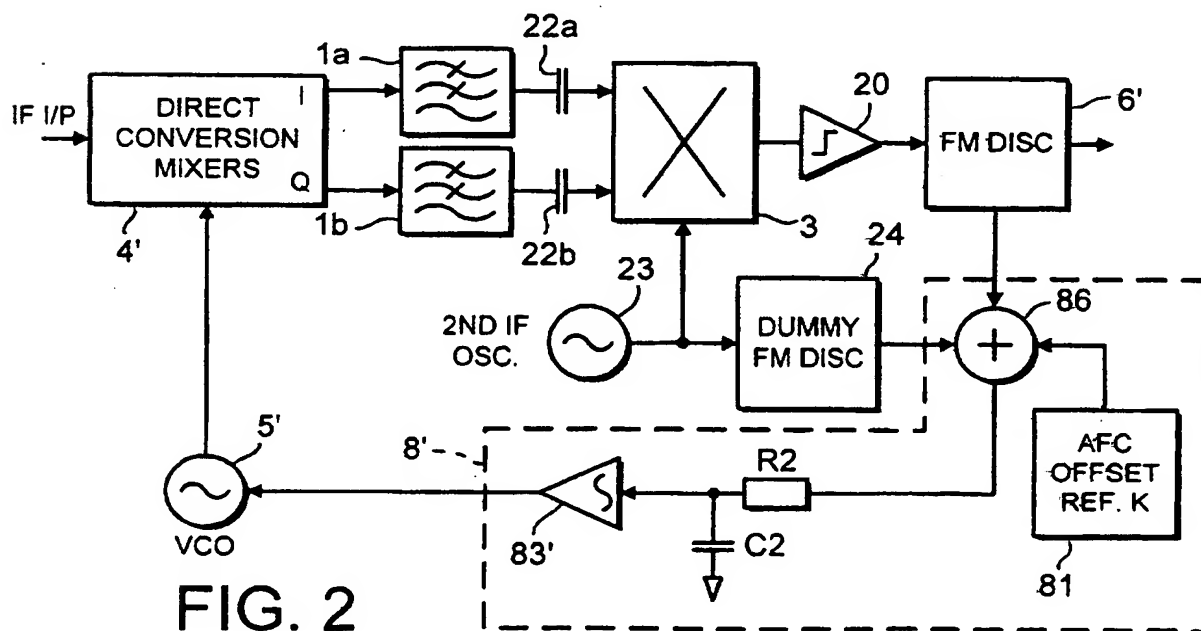
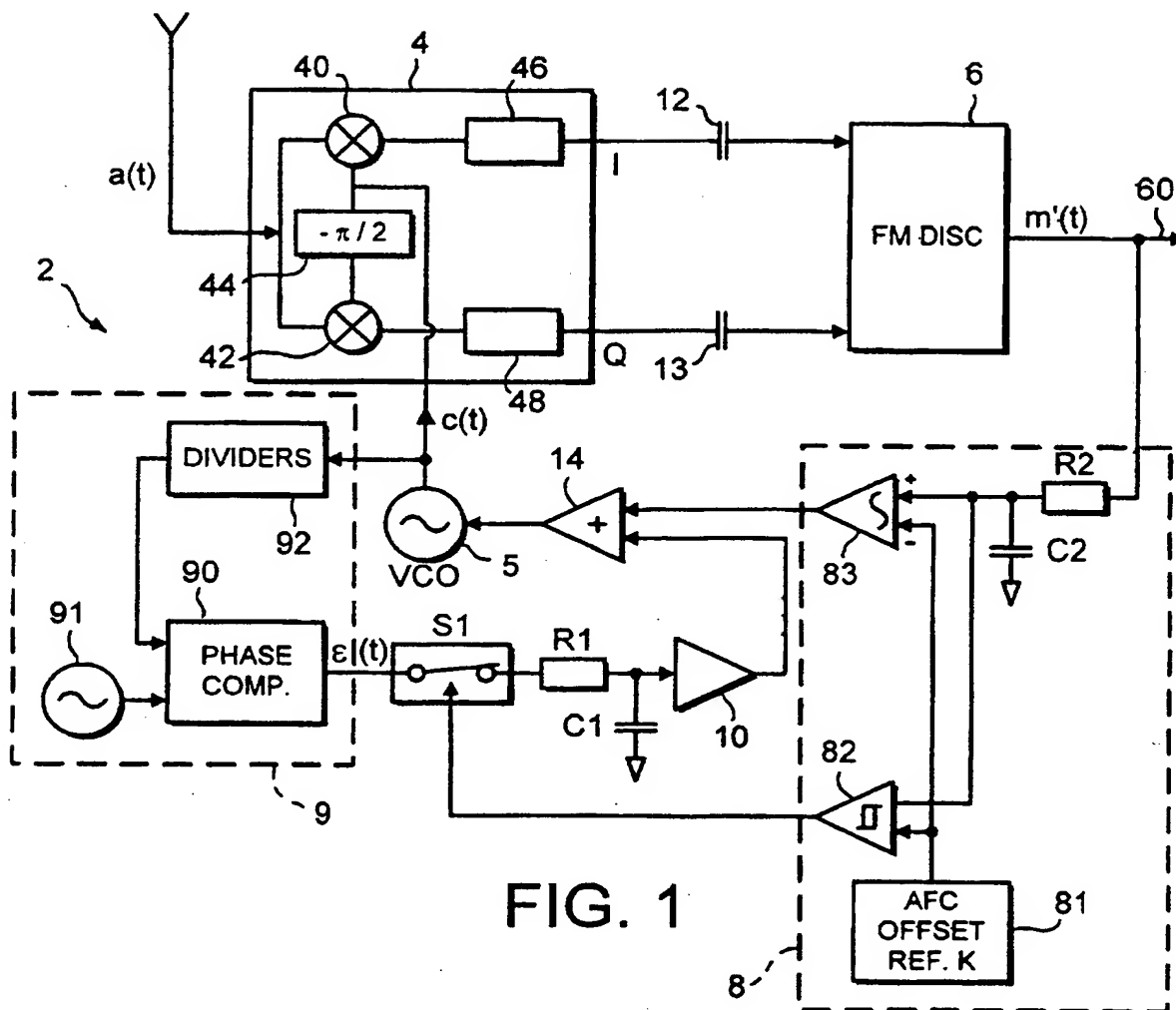


FIG. 1

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.



FM RECEIVER

This invention relates to a Frequency Modulation (FM) radio receiver and in particular to a FM receiver for a portable radio communication device.

A general trend in portable radio communication apparatus is the reduction in volume, weight and power consumption of such apparatus. This has led to efforts towards reducing the number of elements and devices necessary to perform the functions associated with portable communication devices. In particular, the radio frequency front end of portable apparatus, which typically comprises a number of down-converting stages, is an area in which a reduction in the number of elements and devices would be beneficial.

One approach to reduce the number of stages in the radio frequency front-end is to convert a received radio frequency carrier signal down to a DC Intermediate Frequency (zero IF) in a single step. This is termed direct conversion and is carried out in receivers known by any one of the terms homodyne or zero IF receivers, as well as direct conversion receivers. In a direct conversion receiver, received radio frequency signals are converted directly into base band signals, so that separate intermediate frequency stages are not required. Therefore, the number of higher frequency components needed in a direct conversion receiver is less than in conventional receivers which include intermediate frequency stages. Due to less complexity, the degree of integration of direct conversion receivers can be increased compared with receivers which must include intermediate frequency stages.

In FM, a carrier frequency f_c is varied in proportion to a modulating signal $m(t)$ i.e. the signal to be transmitted. The modulated signal comprises an unmodulated carrier term (at the carrier frequency f_c) and various amplitude-

modulated terms (sidebands) centred on f_c . Most of the power resides in a fairly limited bandwidth, centred on f_c .

FM receivers may be used in either analogue or digital devices. The following description will make particular reference to portable radio telecommunication devices such as mobile telephones but the invention is applicable to any device which uses FM modulation.

In frequency modulation, a signal to be transmitted $m(t)$ is modulated onto a carrier signal having a frequency f_c . At a receiver, the modulated signal is generally converted to a DC component and the quadrature signals I and Q. The modulated signal may be initially converted to a signal having an intermediate frequency before being split into its constituent parts DC, I and Q.

A deviation ratio $\beta = \Delta f/f_m$ where f_m is the bandwidth of the signal to be transmitted (e.g. 1000Hz for a test tone) gives an indication of the deviation of the modulated signal from the carrier frequency f_c . In the mobile phone analogue protocol AMPS the normal deviation Δf is around 8kHz for a bandwidth of 1000Hz. β therefore is around 8. In Narrow Band AMPS (N-AMPS) the deviation Δf is around 3kHz for a bandwidth of 1000Hz and β therefore is around 3. The carrier term of the FM signal is therefore much more significant in N-AMPS than in AMPS.

To carry out direct conversion, a local oscillator signal (LO) having the same frequency as the radio frequency carrier signal is mixed with the carrier signal in a suitable non-linear device such as a mixer diode. The output of the mixer contains the sum and difference of the LO and the carrier signal. Thus a mixer output exists at twice the carrier signal, and also at DC (zero Hz). The high frequency mixer output can be filtered by a suitable low pass filter. Once the radio frequency carrier signal has been down-converted, the modulating

signal may be de-modulated using an appropriate demodulator, e.g. an I/Q demodulator for an I/Q modulating signal, or an FM demodulator for an FM signal.

- 5 The local oscillator is typically a voltage controlled oscillator (VCO), the output frequency of which is nominally the same as the carrier frequency of the received signal. It is known to use a Phase Locked Loop (PLL) circuit to tune the local oscillator signal. The PLL produces a resulting error voltage, which is then used to adjust the LO to compensate for any drift in the receiver circuit.

10

In the field of radio telephony, particularly cellular telephony, use of a direct conversion receiver is not without certain drawbacks.

- One of the main problems of using a direct conversion receiver in a cellular radiotelephone, a problem that is widely recognised, is that of unwanted DC in the output of the front-end. These effects are introduced by components of the receiver e.g. amplifiers or unbalanced mixers. The effects basically consist of unwanted DC being provided at the output of the RF front-end stage, which if large enough, causes distortion to the wanted signal. Because
- 15 DC is encompassed in the IF bandwidth, the unwanted DC at the RF front-end output contributed by the IF amplifiers severely limits the sensitivity of the receiver if it is not removed. Low frequency AC such as flicker noise and spurious AM demodulation can also cause similar problems.
- 20

- 25 The dynamic range of the receiver is adversely affected by the fact that, in addition to the high frequency signal of the reception channel, the mixer of the receiver also receives high frequency signals of the adjacent channels, whereby, due to the non ideality of the mixers, a distorting DC signal is produced at the output of the mixer. Thus a stronger signal within the adjacent sidebands can produce substantially higher DC in the signal than the
- 30 desired signal transmitted on the reception channel.

A number of different methods to solve the problem caused by introduced DC effects have been investigated. The most common of these are: AC coupling, closed loop servo correction, and DC averaging and removal.

- 5 AC coupling is the simplest approach. The IF stages are AC coupled which removes the DC voltage and low frequency noise, and stops it from propagating up to the highest gain stages. However it introduces a notch into the centre of the IF pass-band. In the case of modulation such as FM, this results in the carrier term being removed so introducing distortion to the
- 10 required signal, especially for signals having a low deviation ratio β . This is a significant problem with direct conversion: the interference cannot easily be differentiated from the wanted signal. Often a major problem with AC coupling is that the coupling capacitors can take a significant time to charge up which means that the receiver can take tens of milliseconds to settle. Pre-
- 15 charging techniques are typically required. When a narrow band filter is used the settling time becomes long whereby the filter cannot react to quick changes of power. On the other hand with a wide band filter it is possible to achieve a short settling time, but a filter of this kind also filters a substantial part of the useful signal whereby the performance of the receiver is reduced.

20

Closed loop servo-correction has been used in audio amplifiers to remove unwanted voltages. It can also be used in a direct conversion receiver to remove the DC offset created in cascaded IF stages and the mixers. Careful design is required to ensure stability.

25

- DC averaging and removal is usually performed by a Digital Signal Processor (DSP). In this solution, the DC count component of the signal is averaged over a relatively long time frame. The average is then subtracted from the wanted signal. It is broadly equivalent to AC coupling and so can potentially
- 30 introduce distortion. However, it does have the advantage that relatively long average and time (and hence very low cut off frequencies) can be achieved

without the need for high impedance design and/or large value coupling capacitors.

Taking the example of an IQ modulated signal, two consecutive symbols are combined into I and Q signals. Thus I and Q signals are produced from the received signal in an IQ demodulator, on the basis of which a decision is made in the receiver as to which symbol pair (00, 01, 10, 11) has been transmitted. The decision as to whether the transmitted symbol is 0 or 1 is made on the basis on the voltage level of the demodulated signal. Unwanted DC offset can occur in both I and Q signals, which can lead to a wrong decision being made in the receiver as to the signal pair transmitted. In an extreme case, even the error correction logic of the receiver cannot correct the information. In some prior art solutions, an attempt is made to express the signal of the reception channel in spite of high interfering DC offset. However, the drawback of these solutions is the fact that they only operate in situations in which the disturbing DC offset is constant or changes very slowly. In situations in which the powers of the signals in the adjacent channels vary quickly the disturbing DC offset also changes quickly whereby the prior art solutions are not capable of fully eliminating disturbance caused by DC offset. So whilst the prior art solutions are effective in mitigating DC offset in certain circumstances, such solutions do not satisfactorily tackle the problem across a wide range of differing received signal conditions.

According to the present invention there is provided a FM receiver comprising an RF front-end arranged to down-convert a received FM radio signal $a(t)$ having a carrier frequency f_c to a DC intermediate frequency (IF) signal, a local oscillator for providing an output signal $c(t)$ to the RF front-end and a control circuit for controlling the output signal of the local oscillator, wherein the control circuit comprises means for receiving the down-converted signal, means for comparing the DC component of the down-converted signal with a non-zero reference voltage and for outputting a control signal to the local oscillator in dependence on the comparison.

Thus a small frequency offset (eg 50-100Hz) is introduced so that the FM signal's carrier term occurs at this offset frequency and is not within the "DC notch" of the any means, such as AC coupling, used to remove the DC effects introduced by the components of the receiver.

The invention introduces a small fixed frequency offset into a direct conversion receiver's demodulated signal prior to detection which enables distortion caused by DC offset removal circuitry to be avoided. Preferably Automatic Frequency Control (AFC) techniques are used instead of a Phase Locked Loop (PLL) to generate the offset.

Preferably the reference voltage represents a frequency less than 1% of the carrier frequency of the radio signal. Most advantageously the reference voltage represents a frequency less than 200Hz and preferably represents a frequency of 50Hz.

Preferably the receiver further comprises a phase-locked loop (PLL) for providing a coarse-tuning control signal to the VCO, the control circuit being arranged to switch the PLL out of the control loop when the DC component of the down-converted signal is equal or less than the reference voltage.

The local oscillator may be a voltage controlled oscillator.

In accordance with a further aspect of the invention, a method of controlling the output of an FM receiver, the method comprises receiving an FM radio signal having a carrier frequency f_c , mixing the received FM radio signal with a local oscillator signal having a frequency f_i to produce a down-converted signal, comparing the DC component of the down-converted signal with a non-zero reference voltage and outputting a control signal in dependence on the comparison.

In accordance with a further aspect of the invention a control circuit for an FM receiver comprises means for receiving a signal down-converted from a radio frequency to an intermediate frequency, a comparator for comparing the DC component of the down-converted signal and a non-zero reference voltage,
 5 and an output for outputting a control signal in dependence on the comparison.

The invention also extends to a portable radio device incorporating an FM receiver according to the invention.

10

The invention will now be described further by way of example only with reference to the accompanying drawings in which:

Figure 1 shows a first embodiment of a direct conversion receiver according to the invention;

15 Figure 2 shows a second embodiment of a direct conversion receiver according to the invention.

The way of maintaining a small fixed frequency offset for both a synthesised true direct conversion receiver and a direct conversion second IF strip as used
 20 in the latest mobile phone transceivers is described below.

Figure 1 shows a direct conversion receiver 2 having a direct conversion front end 4 for converting the received radio frequency (RF) modulated signal $a(t)$ into the DC and complex polyphase signals I and Q. The direct conversion
 25 front end 4 down-converts the RF signal to zero-IF as a complex (polyphase) signal I/Q. The direct conversion front end 4 is controlled by a LO signal $c(t)$ from a Voltage Controlled Oscillator (VCO) 5.

The RF front end comprises two mixers 40, 42 and a 90° phase sifter 44. The
 30 received signal $a(t)$ is mixed with the LO signal $c(t)$ output from the VCO 5 to produce an inphase signal I and a quadrature signal Q. These signals are then fed to low pass band filters 46, 48 which have a pass band centred on

0Hz with a bandwidth equivalent to the bandwidth of the modulated signal $m(t)$.

The I and Q signals are then AC coupled by capacitors 12 and 13 to remove
5 the DC distortion introduced by the components of the front end 4.

A FM discriminator 6 detects the envelope of the FM signal to produce an output voltage proportional to the instantaneous frequency of the RF carrier within the passband of the receiver. The discriminator 6 has a gain factor of x
10 V/Hz. For example, if the discriminator has a gain factor of 1V/8kHz, an input of 8kHz will produce an output of 1V.

Also provided is an Automatic Frequency Controlled (AFC) offset generator 8 and a PLL 9 for tuning the LO signal $c(t)$.

15

The PLL 9 comprises a phase comparator 90, an oscillator 91 for providing a first reference frequency for use by the phase comparator 90 and a divider system 92. The oscillator 90 provides a signal at a frequency equal to a divisor of the carrier frequency of the signal being received. The divider 92
20 has a value equal to this divisor. The PLL 9 tunes the frequency of the VCO 5 to the carrier (or so-called channel) frequency of the signal being received by the receiver in a conventional manner. Input to the phase comparator 90 are the reference voltage frequency from the oscillator 91 and the output frequency of the VCO 5 divided by the divider 92. The phase comparator 90
25 generates an error voltage $\epsilon(t)$ which is filtered by a loop filter formed by R1 and C1 (buffered by the voltage follower 10). Once the PLL has tuned the VCO so that the signal is within the pass band of the filters 12, 13, the discriminator 6 produces a baseband signal at its output 60. The baseband signal comprises the modulated signal $m(t)$ superimposed on a DC offset
30 introduced by the components of the receiver. In effect, the PLL 9 provides coarse tuning of the VCO output.

The AFC offset generator 8 comprises a filter (R2, C2), an AFC offset reference voltage source 81, a comparator 82 and an integrator 83. The offset reference voltage from source 81 is designed to introduce a fixed offset into the output of VCO 5. This fixed offset represents a very small fraction of the carrier frequency of the received signal. For example, for a carrier frequency of 900 MHz, a fixed offset of 50Hz is introduced (i.e. an offset of $0.4 \times 10^{-6}\%$). The frequency offset introduced is sufficient to move the centre frequency of the modulating signal $m(t)$ out of the bandwidth removed by AC coupling but is not large enough to significantly affect the characteristics of the modulating signal $m(t)$.

The voltage value k can be calculated by considering the gain factor of the discriminator 6. For example, for a gain factor of $1V/8000Hz$, a frequency of 50Hz is equivalent to 6.25 mV. Thus a reference voltage of 6.25 mV will introduce a fixed frequency offset of 50Hz.

Since the receiver may be required to operate at various carrier frequencies, the value of the reference voltage for each carrier frequency may be pre-stored in the receiver and suitable voltage dividers provided to provide the required reference voltages k .

After filtering the output of the discriminator 6 by the filter R2/C2, the filtered output 60 is compared by comparator 82 with the DC reference voltage (k) output from the AFC offset reference source 81. Once the filtered DC offset of the filtered output 60 becomes equal to the DC reference (k), an output signal is produced by the comparator 81. This causes the switch S1 to open which disconnects the PLL 9 from the VCO 5. The PLL 9 is now unlocked and the VCO 5 is under the control of the AFC 8 alone via the summing amplifier 14. The AFC offset generator 8 adjusts the output of the VCO 5 in a fine tuning manner (low gain weighting on amplifier 14) until the AFC voltage across C2 is the same as the AFC offset reference (k). At this point, the

output voltage of the integrator 83 stops ramping and settles to force the output signal of the VCO 5 to the channel frequency plus the required offset k .

5 The PLL may be switched back into the control loop if there is an indication that the output from the discriminator 6 appears to be noisy or the AFC 8 indicates that for some reason the VCO 5 has gone outside the required range. The PLL 9 is reconnected by closing the switch S1. The indication of noisiness may originate from a Received Signal Strength Indicator (RSSI) (not shown) which occurs after the receiver in the signal flow. If the output from
10 the discriminator 6 exceeds the reference voltage k , the output of the comparator 82 will cause the switch S1 to close.

The gain weighting on the input of the amplifier 14 for the PLL error voltage $\epsilon(t)$ is greater than that for the AFC voltage output from the integrator 83 so
15 that the MHz/v for the PLL 9 is greater. The voltage held on C1 when S1 is opened prevents the output of the VCO 5 changing dramatically when the PLL is switched out by switch S1. As the charge from C1 leaks through the input impedance of the voltage follower 10 (which is a very slow process) the voltage from the AFC integrator 83 supplements the VCO control voltage to
20 compensate.

The reference voltage source 81 and AFC loop 8 should be very low noise. The close-in phase noise (eg $1/f$ noise) is normally removed by a PLL. However, when the PLL is disconnected (S1 open) this protection is missing.
25 Some $1/f$ noise will be removed by the AFC action (in effect the discriminator 6 behaves like a low-frequency frequency detector.) However, low noise design is essential to get good receiver performance.

Figure 2 illustrates an embodiment of a dual conversion super-heterodyne
30 receiver in accordance with the invention. An FM receiver system has

integrated channel filters 22a and 22b. The addition of the AFC-locked frequency offset system 8' is shown.

In summary, the principle of the FM processor of Figure 2 is that a first IF
 5 signal (eg 45 MHz) is down-converted to zero-IF (i.e. DC) by quadrature
 downconversion mixers 4'. A VCO 5' provides an input to the direct
 conversion mixers 4' nominally at the first IF frequency. Channel filtering is
 then carried out by low-pass filters 1a, 1b at zero-IF before up-conversion by
 an up-converter 3 to a second IF (e.g. 60kHz). An oscillator 23 provides an
 10 input to the up-converter 3 at the second IF. The oscillator 23 may be a
 simple crystal oscillator or ceramic resonator oscillator which oscillates at, say
 60kHz. At the second IF, the usual limiting and FM detection is carried out by
 the limiter 20 and discriminator 6'. The outputs from the channel filters are AC
 coupled by capacitors 22a, 22b to remove DC offsets which would otherwise
 15 result in carrier leakage from the up-converter 3. In the absence of an offset
 generator 8' according to the invention, this AC coupling would also remove
 the carrier component in the FM spectrum which would result in a large
 amount of audio distortion at the output of the discriminator 6'. This would be
 particularly acute at low deviations.

20

The AFC-locked frequency offset generator 8' in essence moves the centre
 frequency of the FM signal slightly so that the carrier does not fall at DC but
 just outside the notch formed by the AC coupling capacitors 22a, 22b. This
 is achieved by shifting the frequency of the VCO 5' by a very small fraction of
 25 the carrier frequency of the input signal e.g. 50-100Hz. The output from the
 FM discriminator 6' has a mean level which depends upon the frequency
 offset of the IF signal input to the discriminator 6'. A dummy FM discriminator
 24 is used to generate a mean or quiescent output voltage which should be
 exactly the same as that of the primary FM discriminator 6' when there is no
 30 modulation or frequency offset. To this output is added by adder 86 a small
 offset voltage k which represents the desired frequency offset. After lowpass
 filtering by R2/C2 and integration by integrator 83', the AFC correction voltage

is applied to the VCO 5'. Dummy discriminator 24 provides 'calibration' for ambient changes. As temperature and manufacturing variations effect both discriminators, the bulk of the discriminator output voltage is cancelled out so that the correct DC offset is applied to the VCO 5'.

5

Thus the invention overcomes the major drawback of direct conversion radio systems for narrowband or low-deviation FM reception.

10 In a true direct conversion receiver with only one synthesised local oscillator driving the direct down-conversion mixers in the front end, the invention enables the introduction of an offset which is a very small fraction of the receive carrier frequency of the received signal (e.g. 50Hz in 900MHz). In a system which uses a direct conversion second IF, the invention enables the
15 second local oscillator synthesiser to be replaced with a simple crystal or ceramic resonator oscillator without the need for a complicated synthesiser to generate the small frequency offset. No further oscillators or mixers are required.

20

CLAIMS

1. An FM receiver comprising an RF front-end arranged to down-convert
a received FM radio signal $a(t)$ having a carrier frequency f_c to a DC
5 intermediate frequency (IF) signal, a local oscillator for providing an output
signal $c(t)$ to the RF front-end and a control circuit for controlling the output
signal of the local oscillator,

wherein the control circuit comprises means for receiving the down-
converted signal, means for comparing the DC component of the down-
10 converted signal with a non-zero reference voltage and for outputting a control
signal to the local oscillator in dependence on the comparison.

2. A receiver according to claim 1 wherein the reference voltage
represents a frequency less than 1% of the carrier frequency of the radio
15 signal.

3. A receiver according to claim 1 or 2 wherein the reference voltage
represents a frequency less than 200Hz.

20 4. A receiver according to claim 3 wherein the reference voltage
represents a frequency of 50Hz.

5. A receiver according to any of claims 1 to 4 further comprising a phase-
locked loop (PLL) for providing a coarse-tuning control signal to the VCO, the
25 control circuit being arranged to switch the PLL out of the control loop when
the DC component of the down-converted signal is equal or less than the
reference voltage.

6. A receiver according to any preceding claim wherein the local oscillator
30 is a voltage controlled oscillator.

7. A method of controlling the output of an FM receiver, the method comprising
- receiving an FM radio signal having a carrier frequency f_c
 - mixing the received FM radio signal with a local oscillator signal having
 - 5 a frequency f_i , to produce a down-converted signal,
 - comparing the DC component of the down-converted signal with a non-zero reference voltage and
 - outputting a control signal in dependence on the comparison.
- 10 8. A method according to claim 7 wherein the reference voltage represents a frequency less than 1% of the carrier frequency of the radio signal.
9. A method according to claim 7 or 8 wherein the reference voltage
- 15 represents a frequency of 50Hz.
10. A method according to claim 7, 8 or 9 further comprising providing a coarse-tuning control signal from a phase-locked loop (PLL), the PLL being switched out of the control loop when the DC component of the down-
- 20 converted signal is equal to or less than the reference voltage.
11. A control circuit for an FM receiver the control circuit comprising
- means for receiving a signal down-converted from a radio frequency to an intermediate frequency,
 - 25 a comparator for comparing the DC component of the down-converted signal and a non-zero reference voltage, and
 - an output for outputting a control signal in dependence on the comparison.
- 30 12. A control circuit according to claim 11 wherein the reference voltage represents a frequency which is less than 1% of the radio frequency.

13 A portable radio device incorporating an FM receiver according to any of claims 1 to 6.



Application No: GB 9904007.3
Claims searched: ALL

Examiner: Mr. Sat Satkurunath
Date of search: 19 May 1999

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK CI (Ed.Q): H3A: AD, AN, AXB, AXC, AXD, AXF, AXX

Int CI (Ed.6): H03D, H03J, H04B

Other: Online: WPI, JAPIO, EPODOC

Documents considered to be relevant:

| Category | Identity of document and relevant passage | Relevant to claims |
|----------|--|--------------------|
| X | GB2158330 A PHILIPS - see especially figure 16 | 1, 6, 7 and 11 |
| X | US 4944025 GEHRING - see especially figure 1 | 1, 6, 7 and 11 |

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